IN THE CLAIMS

1. (Currently Amended) An image processor, comprising:

image memory ~~which~~ configured to store[[s]] image data;

an image memory control unit, which is connected to at least one connected unit, including at least one of an image reading unit for reading image data, ~~and/or~~ an image processing unit for processing and editing image data, and[[/or]] an image writing unit for writing image data to transfer paper ~~or the like;~~ , and is configured (1) to receive[[s]] at least one of first image data read-in by said image reading unit and~~/or~~ second image data subjected to image processing by said image processing unit[[;]] , (2) to transmit[[s]] at least one of the first image data and~~/or~~ the second image data to said image memory[[;]], and (3) to transmit[[s]] the image data stored in said image memory to at least one of said image processing unit and~~/or~~ said image writing unit;

a system control unit ~~which~~ configured to control[[s]] transmission or reception of control signals used in each of said at least one connected unit[[s]] or between said at least one connected unit[[s]]; and

a source detection unit ~~which~~ configured to detect[[s]] a source of image data received by ~~to~~ said image memory control unit[[;]], wherein

said system control unit is configured to control[[s]] said image memory control unit according to the source of the image data detected by said source detection unit, and to determine[[s]] a transmission order of the image data to said image memory; and

said image memory control unit is configured to control access to the image memory so as to prevent a collision between jobs relating to accesses of the image memory, based on priorities of the jobs.

2. (Currently Amended) The image processor according to claim 1, wherein said image memory control unit is connected to said at least one connected ~~one or more~~ unit[[s]] through an image data control unit[[,]] ; and

~~wherein~~ said image data control unit is configured to perform[[s]] transmission or reception of image data between said image memory control unit and said at least one ~~one or more~~ connected units.

3. (Currently Amended) The image processor according to claim 1, wherein said image memory, said image memory control unit, and said system control unit are configured ~~formed~~ as a discrete controller unit.

4. (Currently Amended) The image processor according to claim 1, wherein said image memory control unit has a bus control unit for controlling a bus connected to said ~~one or more~~ at least one connected units.

5. (Currently Amended) The image processor according to claim 1, further comprising:

an image data compression unit ~~which~~ configured to compress[[es]] the image data; and

a volume determination unit ~~which~~ configured to determine[[s]] whether ~~the~~ an amount of the image data is larger than a predetermined volume,

wherein said image memory control unit is configured to provide[[s]] control[[s]] so as to transmit the image data to said image data compression unit when said volume determination unit determines that the amount of the image data is larger than said predetermined volume.

6. (Currently Amended) The image processor according to claim 1, further comprising:

an image data expansion unit ~~which~~ configured to expand[[s]] the image data; and

a compression determination unit ~~which~~ configured to determine[[s]] whether the image data has been compressed,

wherein said image memory control unit provides controls so as to transmit the image data to said image data expansion unit when said compression determination unit determines that the image data has been compressed.

7. (Currently Amended) An image processor, comprising:

an image reading unit ~~which~~ configured to acquire[[s]] [[an]] image data;

an image processing unit ~~which~~ configured to process[[es]] the image data acquired by said image reading unit;

an image memory ~~which~~ configured to store[[s]] the image data acquired by said image reading unit or the image data processed by said image processing unit;

an image memory control unit ~~which~~ configured to receive[[s]] data sent from said image reading unit or image processing unit, and to receive[[s]] the data sent from said image memory and to transmit[[s]] it to said image reading unit or said image processing unit;

a system control unit ~~which~~ configured to control[[s]] transmission or reception of data by said image memory control unit; and

a detection unit ~~which~~ configured to detect[[s]] which one of said image reading unit and ~~or~~ said image processing unit has transmitted the image data to said image memory control unit,

wherein said system control unit is configured to control[[s]] said image memory control unit based on the detected source of the image data, and to determine[[s]] ~~the~~ an order in which the image data is to be transmitted to said image memory; and

said image memory control unit is configured to control access to the image memory so as to prevent a collision between jobs relating to accesses of the image memory, based on priorities of the jobs.

8. (Currently Amended) An image processor, comprising:

image memory ~~for storing~~ configured to store image data;

an image memory control means which is connected to at least one connected means, including at least one of an image reading means for reading image data, ~~and/or~~ an image processing means for processing and editing image data, and/~~or~~ an image writing means for writing image data to transfer paper ~~or the like;~~ , wherein the image memory control means (1) receives at least one of first image data read-in by said image reading means and/~~or~~ second image data subjected to image processing by said image processing means[[;]] , (2) transmits at least one of the first image data and/~~or~~ the second image data to said image memory[[;]], and (3) transmits the image data stored in said image memory to at least one of said image processing means and/~~or~~ said image writing means;

a system control means for controlling transmission or reception of control signals used in each of said at least one connected means ~~units~~ or between said at least one connected means; and

a source detection means for detecting a source of image data to said image memory control means[[;]], wherein

said system control means controls said image memory control means according to the source of the image data detected by said source detection means, and determines a transmission order of the image data to said image memory; and

said image memory control unit is configured to control access to the image memory so as to prevent a collision between jobs relating to accesses of the image memory, based on priorities of the jobs.

9. (Currently Amended) The image processor according to claim 8, wherein said image memory control means is connected to said at least one connected ~~one ore more~~ means through an image data control means[[,]] ; and

~~wherein~~ said image data control means performs transmission or reception of image data between said image memory control means and said at least one connected ~~one or more~~ means.

10. (Currently Amended) The image processor according to claim 8, wherein said image memory, said image memory control means, and said system control means are configured ~~formed~~ as a discrete controller means.

11. (Currently Amended) The image processor according to claim 8, wherein said image memory control means has a bus control means for controlling a bus connected to said at least one connected ~~one or more~~ means.

12. (Currently Amended) The image processor according to claim 8, further comprising:

an image data compression means for compressing the image data; and

a volume determination means for determining whether ~~the~~ an amount of the image data is larger than a predetermined volume,

wherein said image memory control means provides controls so as to transmit the image data to said image data compression means when said volume determination means determines that the amount of the image data is larger than said predetermined volume.

13. (Currently Amended) The image processor according to claim 8, further comprising:

an image data expansion means for expanding the image data; and

a compression determination means for determining whether the image data has been compressed, wherein

said image memory control means provides controls so as to transmit the image data to said image data expansion means when said compression determination means determines that the image data has been compressed.

14. (Currently Amended) An image processor, comprising:

an image reading means for acquiring ~~an~~ image data;

an image processing means for processing the image data acquired by said image reading means;

an image memory for storing the image data acquired by said image reading means or the image data processed by said image processing means;

an image memory control means for receiving data sent from said image reading means or said image processing means, and for receiving the data sent from said image memory and for transmitting ~~transmits~~ it to said image reading means or said image processing means;

a system control means for controlling transmission or reception of data by said image memory control means; and

a detection means for detecting which one of said image reading means ~~t or~~ and said image processing means has transmitted the image data to said image memory control means,

wherein said system control means controls said image memory control means based on the detected source of the image, and determines ~~the~~ an order in which the image data is to be transmitted to said image memory; and

said image memory control unit is configured to control access to the image memory so as to prevent a collision between jobs relating to accesses of the image memory, based on priorities of the jobs.